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Design A Low Power And High Throughput Error Detection And Data Correction Architecture By Razor II Method

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ABSTRACT

The proposed error detection and correction circuit designed due to the existing circuits accommodate the worst-case delay. To prevent Error in the system, detect and determine violation to maintain correctness to help on the fly mechanisms. The proposed circuit is to present speculative error detection technique along with an error recovery mechanism. Circuits are wanted to oblige the delay and to get to be deficient in their execution. To enhance the execution, they oblige fly system to forestall, identify and correct errors. In this paper, low power speculative error detection and error recovery architecture are

to be developed. The main aim of the circuit is to reduce delay, power and area. This paper demonstrates their ability to operate under worst-case accommodation. The proposed error correction and detection circuit give 226nW, propagation delay 1ps, throughput 792MHz..

1. Introduction

The enforcement of I.C. designers laid a great exertion in diminishing the energy utilization of VLSI systems and suspension gave the inclusive demand for higher speed and more efficient electronics. Circuit and architectural techniques are using the difference in the consumption of VLSI system [1]. Even though the standard method of pipelining is valid and reliable, but the clock frequency is not flexible, and it always stays at the critical path of the framework. In few others, they improve their adaptability to bypass the critical path in the system and more to design. In contrast, other circuit technique focuses more on decreasing the margin to the frequency of the clock because of voltage, thermal vibration, and process. The sources of the changing variant have many different characteristics which can be vigorous to realize. It is essential to understand that diverse variation sources have their attributes which cause Error to be recognized, and recovery methods are utilized [1]. There are two main variations, such as random variation and systematic variation, respectively. Random variation can be a label under static dynamic. Mostly for line end roughness effect and the non-predictable voltage fluctuations could show in unpredictable variation performance. Static random variation is a random dopant fluctuation that gives effect to the transistor threshold voltage (Vth).
Moreover, the dynamic random variations can be voltage vacillations, usually not sure which way the voltage will change, and even though we know how it will change after some time. It is difficult to say how it will precisely influence a specific circuit. The second major of variation is Systematic variations [2]. Systematic variations can adequately describe and displayed as they are indeed known and unsurprising. Sources of variation in CMOS circuits are static variation and dynamic variation. Static variation usually is fabricated dies, which results in more significant power consumption and a maximum frequency of degradation and usually has many problems in sub-100nm technologies. The local and global procedure variation impacts in feature size, the rate of the transistors can shift drastically from dying to die or gadget to gadget. A few planners use procedures to lessen the timing edges and enhance speed. However, others utilize the same methods to spare dynamic energy by diminishing VDD and working at perfect or lower rates. The examination had figure out that minimum energy accomplishes when V_{DD} enters the subthreshold, where can figure out how to attain ten reductions in energy per computation [2]. It

will be harder to anticipate in influential CMOS dies passes on because of the impact of static variations get to be more unsafe [3].
Dynamic variations usually are characterized by the way they fluctuate over the long run. A few sources of variety, for example, supply voltage changes may frequently differ (on the request of a couple of clock cycles) [4] while others, for example, maturing fluctuate over vast times of time for the most part in the quite a long while [5]. Since, their dynamic and hard to foresee nature, it gets to be much harder to plan flexible systems to battle these variations. The first stage of the paper is to identify the design method to design an error detection circuit. The second stage is to locate and designs an error correction circuit. The number of transistors used to design the components must be less to achieve less area occupying design [6-7]. For Error detection circuit Razor 1 circuit is used and modified to produce better circuit. While for error correction hamming theorem and parity bit are used. The third stage of the paper is to simulate and analyze the schematic and the layout of the designs. This finding error stage can separate further into two divisions. The first part will be constructing the schematic of the propose error detection and error correction circuit. The LVS (Layout vs Schematic) simulations carried out on the layout that had been generated to analyze the output results for both error detection and error correction circuit. The results generated from the simulation will be used as the calculation for the outputs such as propagation delay, power dissipation, output power, D.C. power, area efficiency, EPI, latency, throughput and power delay product (PDP). Different kind of sizes will illustrate their advantages in precise output such as voltage and current. The final stage of the papers is to discuss the output results of the simulation. Any drawbacks or limitations of the proposed error detection and error correction architecture are discussed as well.

2. Design methods

Design is the passage through which creativity realized. It is necessary to understand the different aspects of fundamental laws to practical considerations that conduct it. There are some fundamental principles of low power design [8, 9] that are by using the smallest geometry of the highest frequency devices or the lowest possible supply voltage.

2.1 Error Detection Circuit

A Razor I flip-flop circuit is used metastability detection circuits [10]. The configurations of the metastability indicator are expanding process variation because it expected to make a reaction to the flip-flop outputs. Other than that, it additionally obliges the utilization of more significant devices which near to harmful effects of the area and power dissipation of the Razor I flip-flop. So, the additional or included danger of metastability at the *restored* signal that will spread to pipeline control logic, conceivably major to flip-flop disappointment. The micro-architectural domain is to

successfully place the timing issue and design in Razor I, which shown in Figure 1.

Rather than showing both corrections in flip flop and also in error detection, Razor II shows the only detection in flip flop. Still, the correction in it is an architectural replay [11]. Although the price of the IPC penalty gets higher during recovery, these allowed the complication and the size reduces Architectural replay is a conventional method that consists of better performing microprocessors to help in the operation, for example, out-of-request execution and branch prediction. Besides, that is easy to overwhelm the remaining framework, which helps recap in the timing errors event. These methods need for pipeline *restore* signal, whereas expressively unwinding the timing imperatives on the error-recovery way [12]. This Razor II characteristic is agreeable to utilize in better-performance processors.

The procedure of Razor II flip-flop comprises a positive level latch contrast with the master-slave flip-flop [13]. It describes that any changes on the input information of the decisive clock stage with timing mistake. Rejection of master latch expressively brings down the clock-pin limit by reducing its energy furthermore overhead area. Other than that, it additionally offers the opportunity to the Razor II flip-flop to regularly find the Single Event Upsets (SEU) sensibly and registers without the overhead. So, it gives lower area value [14].

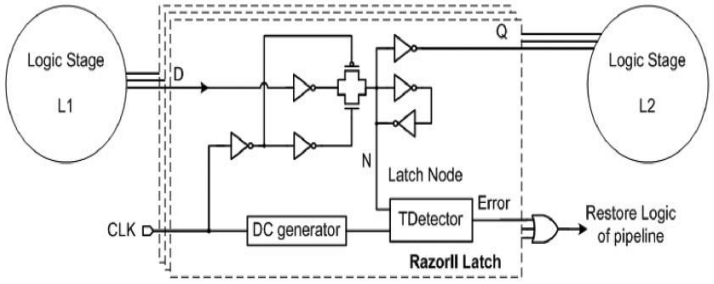

Figure 1*: Razor II Flip Flops*

The main text starts at the top of the page and continues in a Errors are recognized with watching changes to the output of the latch all through the higher clock stage if information transitions happen through the higher clock stage. The transition detector utilizes a progression of inverters joined with transmission gates to produce a progression of beats that stand like the inputs to a gate or element [15]. The detection clock will discharge the yield node, and an error hailed if the information reaches after the starting time of the latch. Besides, the data path flip-flop is replacing from Razor with the use of level latch evacuate the requirement for metastability detection circuit. On the off chance that the metastability detector and master-slave flip-flip eliminated. Razor II would show enhanced area and also power over Razor I.

2.2 Proposed Error Detection Circuit (Razor II)

Figure 2 shows the detection clock generator, and Figure 3 shows Razor II flip-flop transition detector. The transition-detector as demonstrated in Figure 3 uses a delay-chain to produce a 'verifiable' beat out of an increasing and a decreasing transition at latch node which is N. The beat is after that caught from a component OR gate to deliver the error signal. Two beat generators are obliged to notice the changes in both headings. The AND gates needed for the production, that gathered with the piece of the assessment value [16]. A valid sample is the best generator for the increasing transitions at node N, uses the inverter, I_3, and the transmission gate, TG2, to make obliged delay. The nodes are D_1, and D_3 are the inputs of the comparing AND gate, as shown in Figure 3.

Additionally, the beat generator for the decreasing transition uses gates I_2 and TG1. Here D0 or D_2 is the comparing AND gate. For specific purposes, the delay chain for every beat generator guarded by changing the TG1 and TG2 in the delay chains through the TD-TG V_{DD} pin.

The error reset signal is pre-charges the variable hub in the OR-gate to catch consequent moves on the latch hub. The reset created when design recovery on account of a timing error. With the use of reset motion rather than a clock for pre-charge lessens the total clock-pin capacitance [17]. In this way, the variable hub is restrictively pre-charged in the midst of recovery, on account of a timing error. A cross-coupled inverter pair is used as a hook structure to shield the variable hub from discharge because of spillage.

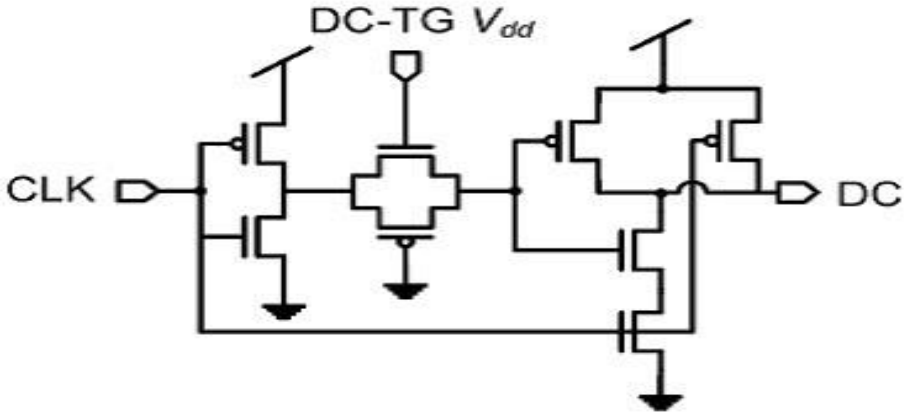

Figure 2: *Razor II Detection Clock Generator*

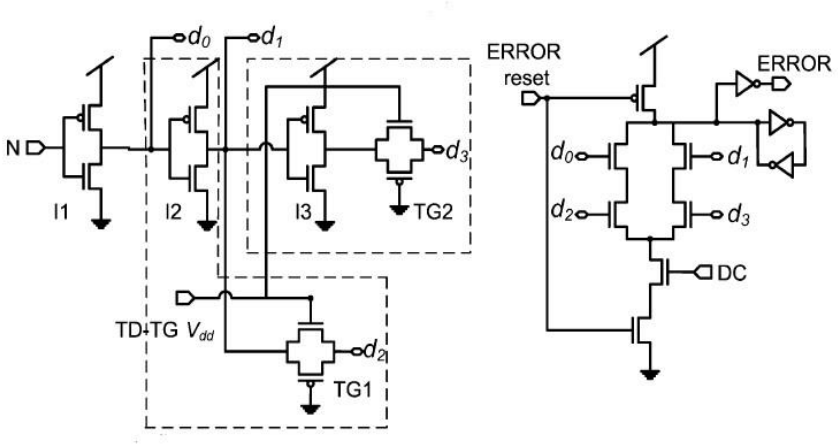

Figure 3: *Transition Detector in Razor II*

At the point when utilizing Razor II circuits, this is essential to be known of the exchange offs that exist in attaining to right uses of timing window that permit Razor II to check errors effectively. If a short route exists in the combinational rationale and it reaches the error signal before the clock-edge of the computation an existing it, a wrong error can trigger. To, right this; buffers are embedded in the agile approach to verify that each way can be accurately gotten [18]. The razor II circuit can ensure a base timing limit (hold time) of the shadow latch met. However, inserting buffers likewise prompt extra power and area. Razor II circuit designed in the VLSI CAD tool platform. However, several gates created using PMOS and NMOS to make sure highly efficient with lower delay. The diagram of the designed Razor II circuit shown in Figure.4.

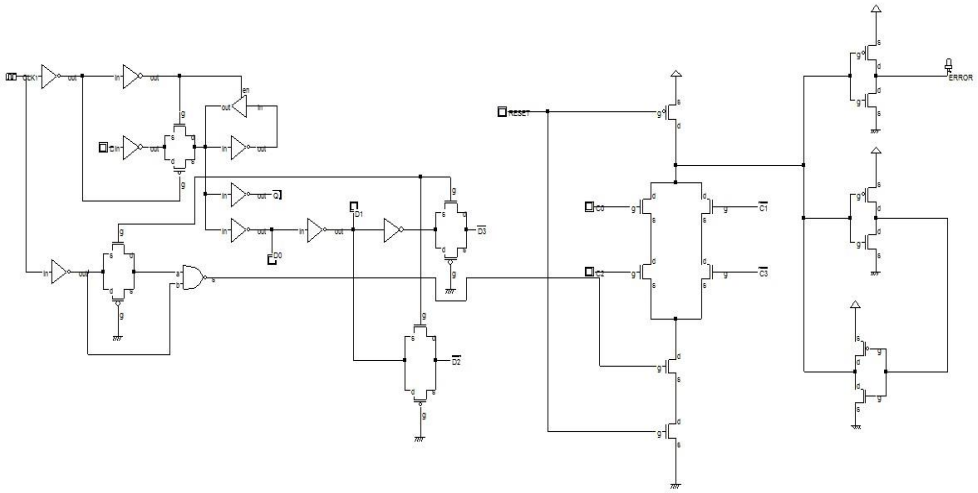

Figure 4: *Razor II Proposed error detection circuit*

From the circuit, data bit D0, D1, D2, D3 are used to identify errors while check bit C0, C1, C2, C3 are used to correct the errors. Once the Razor II circuit designed using the stated method, it's verified with button and lamp.

The area of the Razor circuit is 0.644nm. The numbers of transistors are 17 NMOS and 31 PMOS.

2.3 Proposed Error Correction Circuit

When the Error is detected, a particular form of procedure needed to approach for the Error noticed to be handled systematically and in a proper manner. This section describes the design and implementation of the proposed error correction circuit. A one-bit comparator circuit used in this architecture. The comparator circuit compares the two bits and gives high output if A bit greater than B bit, which is known as **F= AB'**. The proposed Error Correction Circuit show in Figure 5. The design obtained using the DSCH2 method, as stated earlier. The circuit uses three NOT gate, six AND gate, four OR gate and two 2-to-1 Multiplexor circuit to give the output logic. The MUX takes in 2 input to produce the cumulative output data with the help of the selection input, either logic "1" or logic "0". The MUX designed in order of selection input and its complement. The output of the MUX circuit is one of its inputs [18]. A 2-to-1 multiplexer Boolean equation shows in Equation 3.1. Where A and B stands for the two inputs, selector input is S, and the output gives as Z:

$$Z = (A.\bar{S}) + (B.S) \quad (1)$$

As shown in Figure 4 proposed error correction circuit, the error correction inputs are given in the input sector of *a0, a1, a2* and *a3,* respectively. It can be feed either logic low or logic high. These four inputs are data bits or error bits stream for the circuit. Then, the data bits pass into one bit 2-to-1 comparator circuit. The error bits stream is compared by two bits consequently. Using the given data bits, the A greater than B one-bit comparators compare the first value with the second value, which is in sequential order. The circuit is because the error bits maybe one or zero in the logical terms. If A is greater than B in logical wise, the comparator circuit gives logic "1" otherwise logic "0". According to the parity check, the comparison has done from a higher value to lower value. After that, the comparing values sent to the two-input OR gate as one of the inputs.

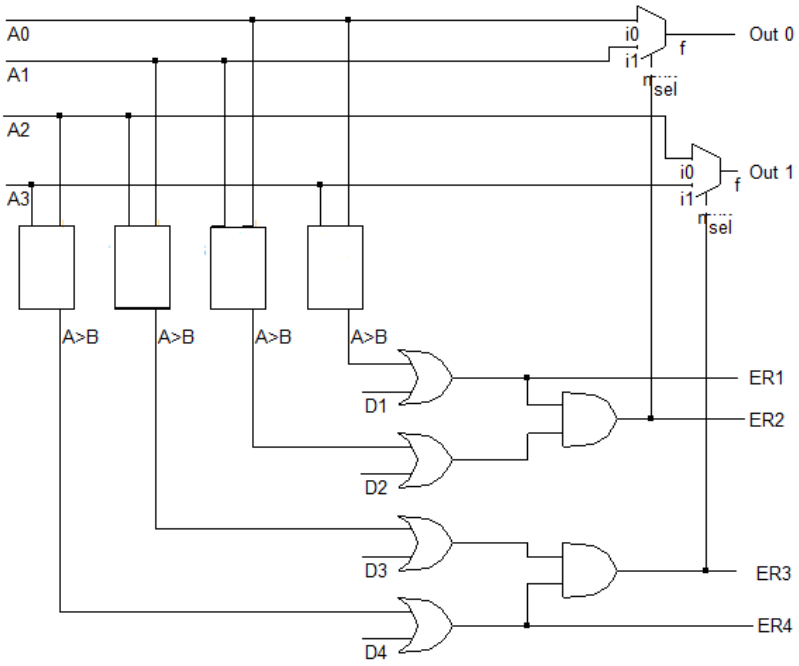

Figure 5: *Proposed Error Recovery Architecture*

The correction bits D_1, D_2 D_3 and D_4, are feed into the second input of OR gate. The correction bits also called check bits. The OR gate value corrected by check bits depends upon comparison results. Then, all the output values from the OR gate passed through two AND gate as a correct value. The MUX circuit uses the corrected gate output to produce the cumulative output data. The corrected gate output again feeds into selection input of multiplexer circuit which is to correct on original outputs.

The designer is using the error recovery method, the Error Detection circuit designed. This section explains the design and implementation of the proposed error detection circuit, which is Razor II and proposed error correction circuit.

3. Results and discussion

This results and discussion section are the continuous development and design of the proposed system, which deals with the experimental views of the Error Correction Circuit and Razor II. In the previous section, the details of the circuits are explained statistically. As per design methodology, test bench created and proved using unknown and known output values of the test bench. The circuit explained in two paths that are layout level and circuit-level simulation.

3.1 Validation Process and Simulation Results

The proper VLSI CAD tools check the validation of the corresponding output and output validation of the inputs and after that verified schematic and the layouts. This CAD tool performs an analysis of the digital

characteristics such as output voltage, output power, average current power delivered in the component, power dissipation, total chip area, propagation delay, Energy Per Instruction (EPI), Power Delay Product (PDP), latency and throughput used in the proposed circuits. The experimental details of the correction circuits and proposed error detection explained in the following sections.

3.2 Proposed Error Detection Circuit – Simulation Results (Razor II)

In Figure 6, it shows different input patterns are tested for the circuits, and the design does satisfy the functionality of the Razor II. When the given check bit is similarly, there will be no error while the check bit in series produces errors and need to be corrected from the timing diagram [18]. Q and D is a button from D flip flop design. When the data bits are enabled, and the no error bit are enabled. According to correction bit, the errors rectified whenever the data bits are enabled, whenever the reset is used to bring the circuit to the original state so that the results will not be overlapped.

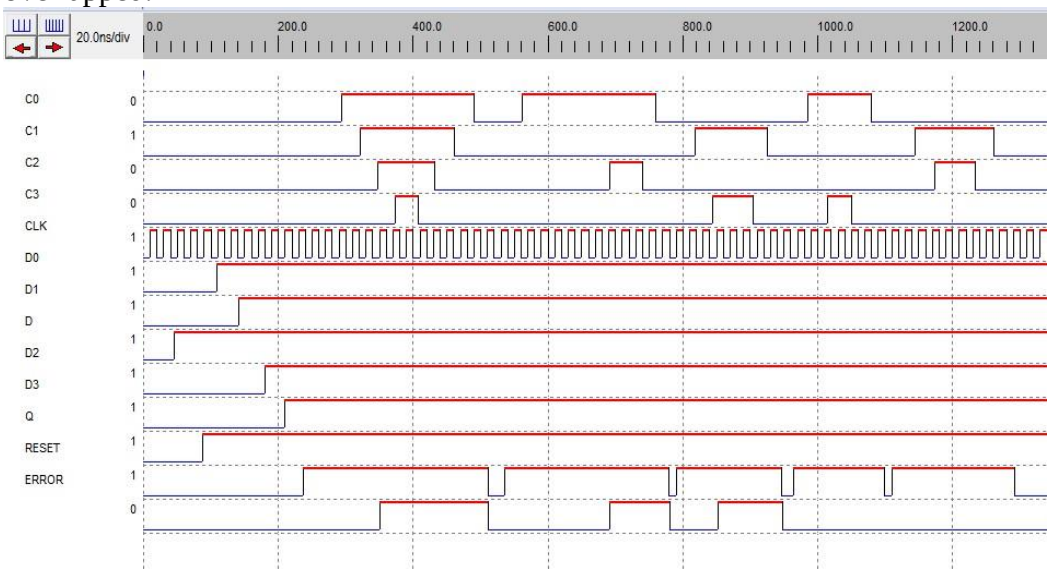

Figure 6: *Timing Diagram of the Proposed Error Detection Circuit*

The projected Razor II imposed into Layout VS Schematic (LVS) simulation for different input patterns. We implement the design with VLSI CAD tool to evaluate the performance of this low power multiplier for different feature sizes of CMOS design rule technology. The final results and simulation results of performance for the four feature sizes are given in Table 1. The other performance parameters, namely Latency, Energy per Instruction (EPI), and Power Delay Product (PDP) calculated, and the results have been tabulated in table 1.

The LVS has measured for different feature size. According to table 1, the 65nm feature size has given a better performance than other feature sizes. The CMOS 65nm feature size provides power with dissipation is 1.50µW, which is achieved in 51.6%, 58.21%, 90.58% than 90nm, 120nm and

180nm feature size, respectively. Similarly, the propagation delay, chip size, EPI, latency, throughput and PDP than other feature sizes. The error correction circuit achieved than other existing circuits. The proposed circuit has the lowest power dissipation, lower total chip area and lower power delay product. It achieves the aim of the paper, which is to achieve circuit with low power, small area and low delay.

Table 1: *The simulation results and performance analysis results of Proposed Razor II*

Output variable	Proposed Razor II (Feature size)			
	65nm	90nm	120nm	180nm
Output Voltage, Vo(V)	0.689	0.992	1.193	1.978
Average Current, (mA)	0.265	0.389	0.484	0.724
Output Power, Po(µW)	252.0	389.0	581.0	1448.0
P_D (µW)	1.50	3.10	3.59	15.928
td(ps)	1.25	2.57	2.91	3.5
Area($\mu m^{2)}$	517	638	767	2716
EPI (fJ)	18.90	39.75	62.57	186.59
Latency, T(ns)	19.01	20.02	20.08	20.06
Throughput, R(G)	0.209	0.1998	0.1995	0.1994
PDP (fWs)	4500	3100	3590	1592.8

Figure 7 is shown the LVS graph of voltage vs time obtained from the simulation of the proposed Razor II, which measure between sum and input gives a more excellent performance. For the feature size 65 nm, the output voltage from Figure 7 is 0.689V. Based on the NMOS technology, the output needs to be VDD /2 for linear operation [19]. This proposed error detection gives higher output voltage that is more than a linear region voltage due to the actual arrangement of NMOS transistors and reduced critical path in the circuit. The critical path increases the parasitic capacitance is reduced, therefore decreases the delay of output (spike). There is no transition delay between the output data (spike).

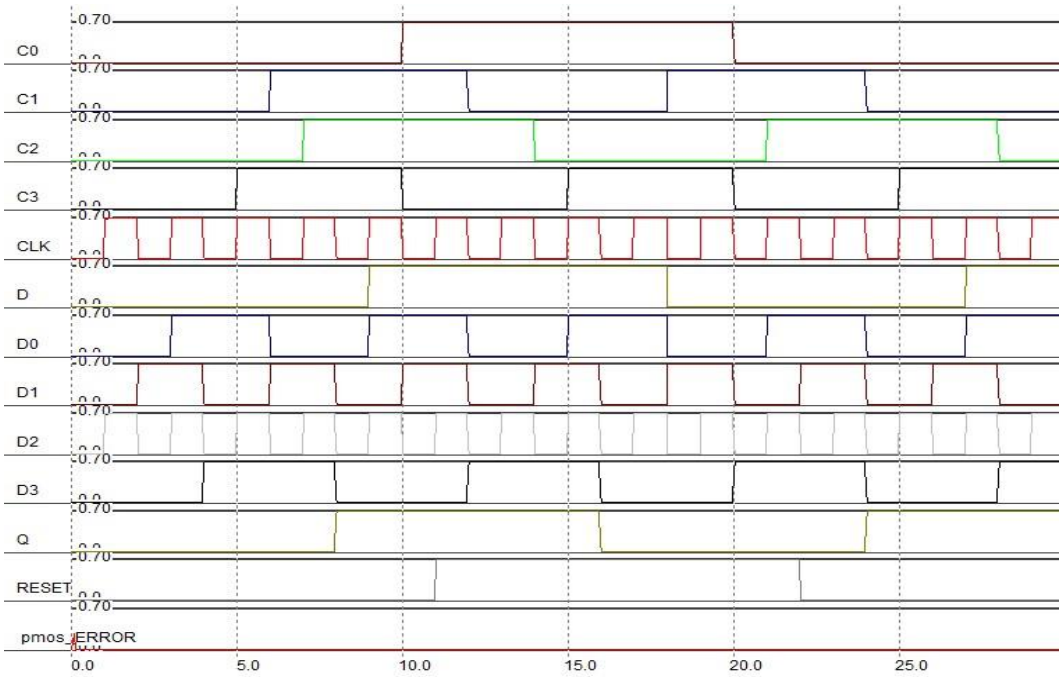

Figure 7: *LVS graph of Voltage vs Time of the Proposed Error Detection Circuit of Feature Size 65nm*

3.3 Analytical Results (Razor II*)*

After getting a layout simulation from CAD tools, we use parametric analysis to get a relationship of output voltage with power dissipation (mW), final voltage (V) and maximum IDD current (mA) using *Error* as an output. For 65nm, the dissipation power is increased with the voltage. The power dissipated for zero voltage is 0.290mW. For 90nm, the dissipation power is slightly increasing with the voltage. The power dissipated for zero voltage is 0.430mW. For 120nm, the dissipation power is slightly decreasing with the voltage. The power dissipated for zero voltage is 0.600mW. For 90nm, the dissipation power decreases with the voltage. The power dissipated for zero voltage is 3.250mW.

3.4 Proposed Error Correction Circuit

The input is given here is A0, A1, A2 and A3 according to the truth table. The input is passing through two bits comparator to check higher value (A>B). The bits are corrected by check bits and feed into multiplexor circuit to produce actual output. From Figure 8, we can see that A0 and C1 are related to ER1. Same goes to A1 and C2 to ER2, A2 and C3 to ER3 and finally A3 to C4 to ER4.

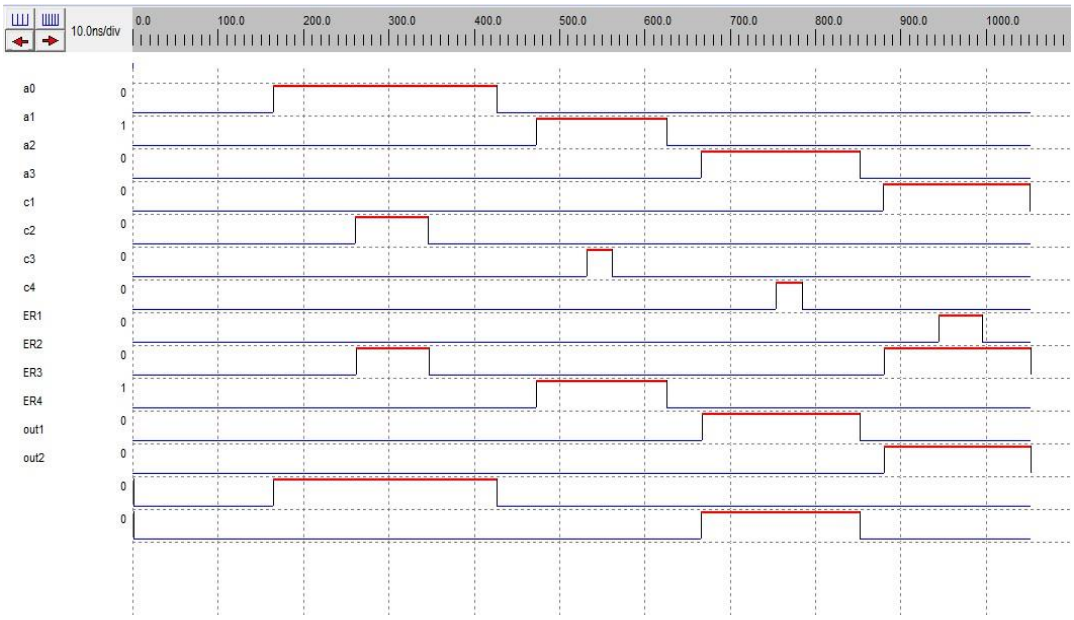

***Figure 8**: Timing Diagram of the Proposed Error Correction Circuit*

With the use of the DSCH2 platform, we construct a 4-bit truth table using A0, A1, A2 and A3 as input. The truth table is shown in Table 2., which used for checked with hamming code technique. The error bit has to be given an unwanted error signal due to unfit in the system.[22] The noise or unwanted disturbance in the circuit the original bits are received in the form of Error. The X-OR technique to both bits of output and correct the error bit to the original bit.

***Table 2:** Truth Table from Error Correction Circuit*

Inputs				Outputs					
A_3	A_2	A_1	A_0	O_1	O_2	ER1	ER2	ER3	ER4
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0
0	0	1	0	0	0	0	1	0	0
0	0	1	1	1	0	0	0	0	0
0	1	0	0	0	1	0	0	1	0
0	1	0	1	1	1	0	0	0	0
0	1	1	0	0	1	0	1	0	0
0	1	1	1	1	1	0	0	0	0
1	0	0	0	0	0	1	0	0	1
1	0	0	1	1	0	0	0	0	1
1	0	1	0	1	0	1	1	0	1
1	0	1	1	1	0	0	0	0	1
1	1	0	0	0	1	1	0	1	0
1	1	0	1	1	1	0	0	1	0
1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	1	0	0	0	0

The proposed error recovery circuit further imposed to Layout VS Schematic (LVS) simulation for various input patterns. Then, the results obtained from the simulation, followed by an analytical discussion of the results were shown in table 3. The performance of this low-power circuit has implemented the design with VLSI CAD tool for different feature sizes of CMOS design rule technology to evaluate the results. The simulation results and calculated results of performance for the four feature sizes are given in Table 3.

Figure 9 shows the LVS graph of voltage vs time obtained from the simulation of the proposed Razor II layout for feature size 65nm. The LVS graph of voltage vs time measure between input and sum gives a better outperformance. It also shows output voltage for the respective feature size. According to NMOS technology, the output must be VDD /2 for linear operation. This proposed error detection gives better output voltage that is more than the linear region voltage due to the proper arrangement of NMOS transistors and reduced critical path in the circuit. This kind of arrangement in the proposed circuit the parasitic capacitance values are reduced, therefore decreases the delay of output (spike). The transition delay increases when the feature size is increase due to the area size. Using the LVS graph of voltage vs time, we can get the output voltage for the respective feature size.

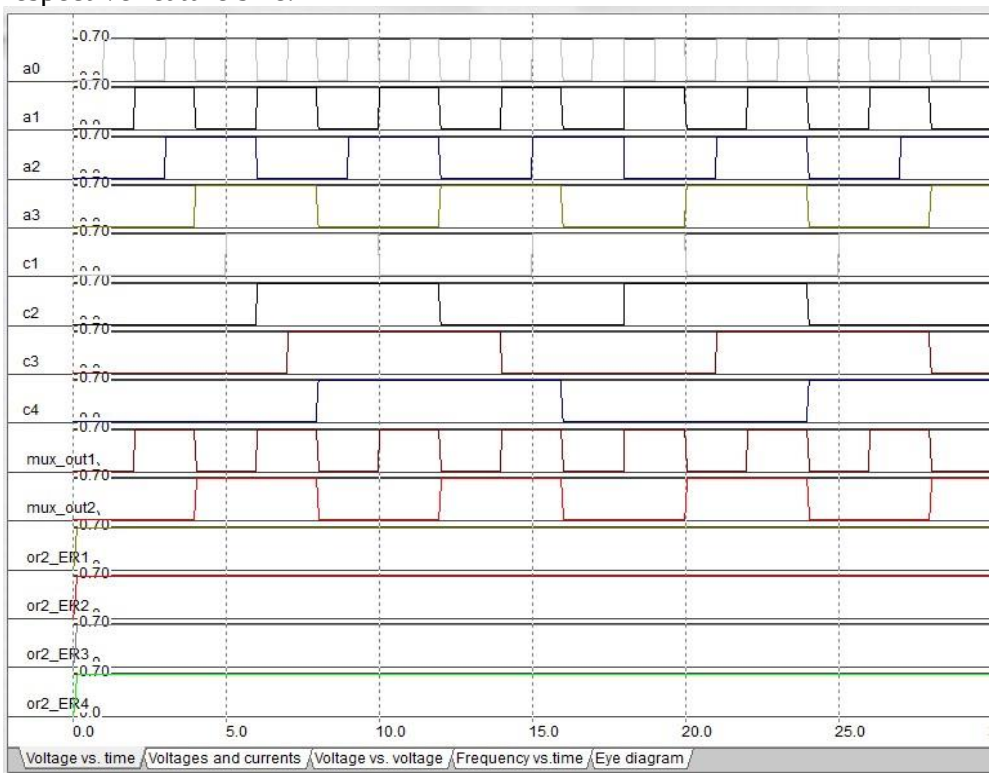

Figure 9: *LVS graph of Voltage vs Time of the Proposed Error Correction Circuit of Feature Size 65nm*

The values for the designed Error Correction circuit are taken from the layout structure. The analyses are made for the in-depth sub-micron process. The result obtained for the 4 CMOS technology fixture size is summarized in Table 3. The Ultra Deep Sub Micron (UDSM) feature size (180 nm, 120 nm, 90 nm and 65 nm) simulated results are shown in Table 3.

For the feature size of the 65 nm, the output voltage is 0.696V. It is calculated from Voltage vs Current graph. The corresponding output voltage for 90 nm, 120 nm and 180 nm is 1.001V, 1.197V and 1.988, respectively. Simulation layout results check the Average Current and Output Power. The 65 nm feature size gives the lowest average current while 180nm gives the highest average current due to transistor channel complete. The delivered power is calculated using the standard equation. For 65 nm, the output power dissipation 0.226µW is calculated from subtracts the value of total power of the circuit and power delivered in the component (output node) of the circuit. Therefore, the output power dissipation obtained for the corresponding technologies is 0.298 µW, 0.126 µW, and 1.972 µW, respectively. Feature size 120nm gives the lowest value of power dissipation. The circuit signal propagation delay is measured from the output signal of the designed error detection circuit, correspondingly the rise time and fall time of the output signal. The propagation delay acquired is 1ps for all the four technologies.

Table 3 also illustrates the total area of the designed gate. The total chip area has been calculated in terms of transistor area, interconnect area, wire area, input and output pad area. For the 65 nm CMOS technology feature size, PDP is 0.226 fWs. The results obtained for the corresponding CMOS technology feature sizes are 0.298 fWS, 0.126 fWS and 1.972 fWS, respectively. The overall best feature size for the proposed error correction circuit is CMOS technology 65nm. It achieves the aim of the paper, which is to achieve circuit with low power, small area and low delay.

Table 3: *The simulation results and performance analysis results of Proposed Error Detection Architecture.*

Output variable	Proposed Error Detection Architecture (Feature size)			
	65nm	90nm	120nm	180nm
Vo(V)	0.696	1.001	1.197	1.988
I_{DD}Avg(mA)	0.002	0.008	0.013	0.081
Po(µW)	1.618	8.306	15.687	163.0
P_D (µW)	0.226	0.298	0.326	1.972
td(ps)	0.896	0.916	1.562	8.963
Area($\mu m^{2)}$	330	385	738	2349
EPI (fJ)	19.29	40.473	62.993	2349
Latency, T(ns)	5.051	5.012	4.999	5.008
Throughput, R	0.792	0.798	0.800	0.799
PDP (fWs)	0.226	0.298	0.126	1.972

4.3.1 Proposed Error Correction Circuit – Analytical Results

Parametric analysis from VLSI CAD tools is used to get a relationship of output voltage with power dissipation (mW), final voltage (V) and maximum IDD current (mA) using multiplexer circuit *Out1* as an output. The parametric analysis is used for all four-feature size 65nm, 90nm, 120nm and 180nm to find the difference between them. The proposed circuits satisfy the equation power (P) equal to the voltage (V) multiply current (I), P = IV. Power is directly proportional to voltage. For 65nm, the final voltage is slightly decreasing with the increasing output voltage. The final peak voltage is at 0.4 VDD with value 0.325V. For 90nm, the final voltage graph is decreasing until 0.2VDD and increasing after that exponentially [23]. The final peak voltage recorded at 0.6 VDD with value 0.625V. For 120nm, the final voltage graph is rising to 0.5 VDD and decreasing after that. The final peak voltage is at 0.5 VDD with a value of 0.650V. For 180nm, the final voltage is slightly increasing with the increasing output voltage. The final peak voltage is at 0.8 V_{DD} with value 0.890V. For all the four-feature size the max IDD current is increased with the voltage. Voltage is directly proportional to current. The graph gets steady after 0.6V. For 65 nm. For 90 nm, the chart gets steady after 0.4V. For 120nm, the chart gets steady after 0.6V. While for 180 nm, the graph gets steady after 0.6V.

In summary, max IDD current stabilize after 0.40 to 0.60 output voltage of respective feature size. For 65nm, the graph increases first then decreases until it achieves a secure frequency value. The stabilize frequency node is at 0.164 GHz. For 90nm, the graph falls first then grows until it meets maintain frequency value. The stabilize frequency node is at 0.202 GHz. For 120nm, the graph increases until it achieves maintain frequency value. The stabilize frequency node is at 0.164 GHz. For 180nm, the graph increases and decreases until it reaches preserve frequency value. It shows there is an unwanted impulse at the starting value of the graph. The stabilize frequency node is at 0.162 GHz. In summary, the frequency node gets maintain after a specific output voltage of respective feature size.

4. Conclusions

The main aim of this paper is to design low power error detection and data correction architecture. The error correction and detection circuits are Razor II circuit proposed and simulated. The proposed error detection and error recovery architecture show a significant improvement in terms of power dissipation, area and Energy Per Instruction (EPI) value. Apart from the reduction in low power, low area and low delay are also achieved. Theoretical systems give a better description of circuit delay with acknowledged timing to enhance throughput or possibly hypothesize timing impelled errors. Usually, error detection and data recovery can be a dispute, mainly when working under a sub-threshold region. The essential strategies that accepted will keep on being utilized. In the futures, a well-designed

Razor Circuits gives lower power dissipation less occupying area and the Multiple Issue using the pipeline technique that matched with higher-level techniques, for example, error-correcting codes

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