PalArch's Journal of Archaeology of Egypt / Egyptology

REVIEW OF EMERGING TRENDS IN LOW POWER MULTIPLER

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Sheetal Nagar, Seema Nayak,Govind Singh Patel: Review Of Emerging Trends In Low Power Multipler -- Palarch's Journal Of Archaeology Of Egypt/Egyptology 17(9). ISSN 1567-214x

Keywords: Low Power Design, Wallace, Dadda, Speed, Area.

ABSTRACT

A significant amount of power is consumed by multipliers which in turn results in lowers processing speeds. In this paper we review and investigate the use of low power multiplier to resolve the issues of various applications such as Artificial Intelligence, Machine learning , IOT(Internet of thing), FIR, IIR, DSP and Image processing, multimedia/signal Processing, patter recognition or Image Shrinking and data mining and analysis. Various Schemes and different architectures of low power Multiplier are Analyzed or Compared for betterment of the parameters like Area, Speed, Energy, Power and Delay. Various Tools used for the simulations like Mat lab, Xilinx and Verilog.

1. Introduction

In today era low power consumption on a integrated circuit has been high for accurate calculations and power issues[1]. Inexact (Approximate) computing is highly recommended to solve the power issues and error tolerant issues [2]. Portable devices and minimization of size always demand of the market which attract the researchers toward the [3] multiplication techniques. Popular applications of low power multiplier in human perception, DSP, machine learning, artificial intelligence , IOT and

pattern recognition [4] Inexact (approximate) technique used for various levels like in circuit of the ICs, architecture of Microprocessors and correlations [5,6]. Polyphase filter banks are the applications of DSP [7] for decimation or interpolate ion [8] which are basic block in conversion of sampling rate [9] . Multiplication has error tolerant Applications [10].

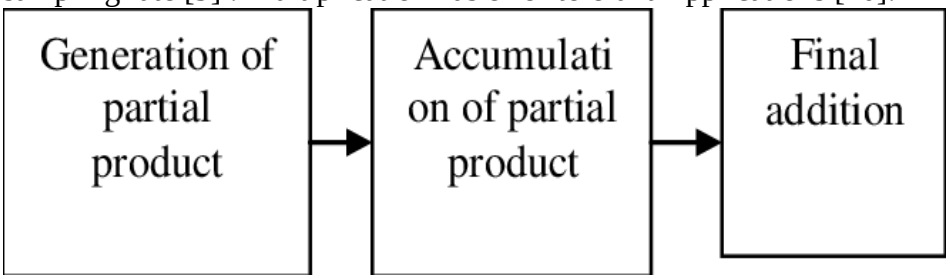

Figure 1 *Conventional Wallace tree Multiplier*

Basic block diagram of Conventinal Wallace tree multipler are shown in the figure 1. Wallace tree multiplier have three basic blocks for Multiplication. Which are generation of partial product , output of partial product will be served as input to the Accumulation and final block contain the Final addition.

A versatile multimedia functional unit can be design using low power parameters i.e multiplication, subtraction, addition interpolation, SAD and MAC using various configuration [11] SPST for VMFU with decrease dynamic power can be reduce with the capacitance switching minimization can be analyzed [12] and design [13] presents multiplier with dynamic range determination unit with booth codes for power saving . In Architecture design of Multiplier with SPST modification can be done with both encoder [11].

Minimization of no of full adder and half adder with reduction of tree [14] design can be used to partial product rounding consider with the deletion, truncation and reduction. To reduce the area cost truncated multiplier can be design [15-18] or fixed with multiplier [19-24].

Computation Accuracy and precision of absolute error [14] in truncated multipliers have application in the field of function Evaluatoion.16x16 bit single cycle 2's computers multipliers [25] use CMOS technology with fabrication on 90-nm dual Vt and frequency 1GHz with the 9mw power.

Reduction in the bit with 2's compliment in multipliers are the main component of the DSP execution cores and Accurate Embedded processor [25].Multiplication is the integral part of such application like FIR filters, IIR filters, DCTs, DSP and FFTs. These require energy efficient multiplier. To reduce the No of inputs N with the counter which convert 3iIP into 2 output in Wallace tree multipliers using log(N/2) levels of the counter [25].Figure 2 shows the Wallace booth Multiplier. In which booth algorithm and compressor are used. 3.2 compressor on first stage, 4.2 compressor on second stage and 5.2 compressor on third stage. These compressor are replaced with full adder.

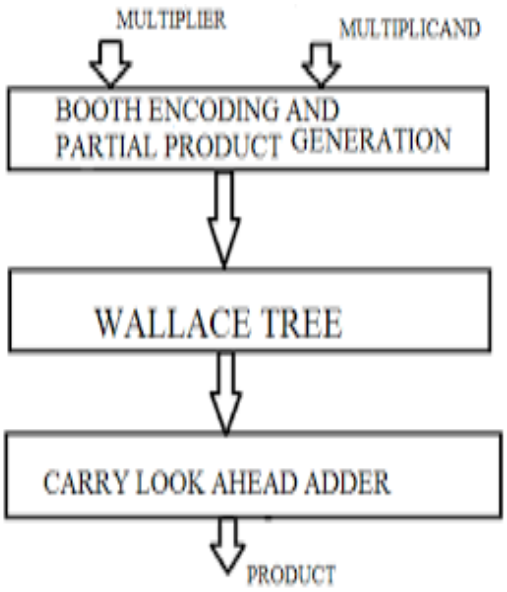

Figure 2 *Wallace Booth Multiplier.*

In Dadda multiplier compression of the counter member using in trees in minimized .This tree reduce no of bits and simplicity the Internal routing in the multiplier this reduction can lead Delay improvements.

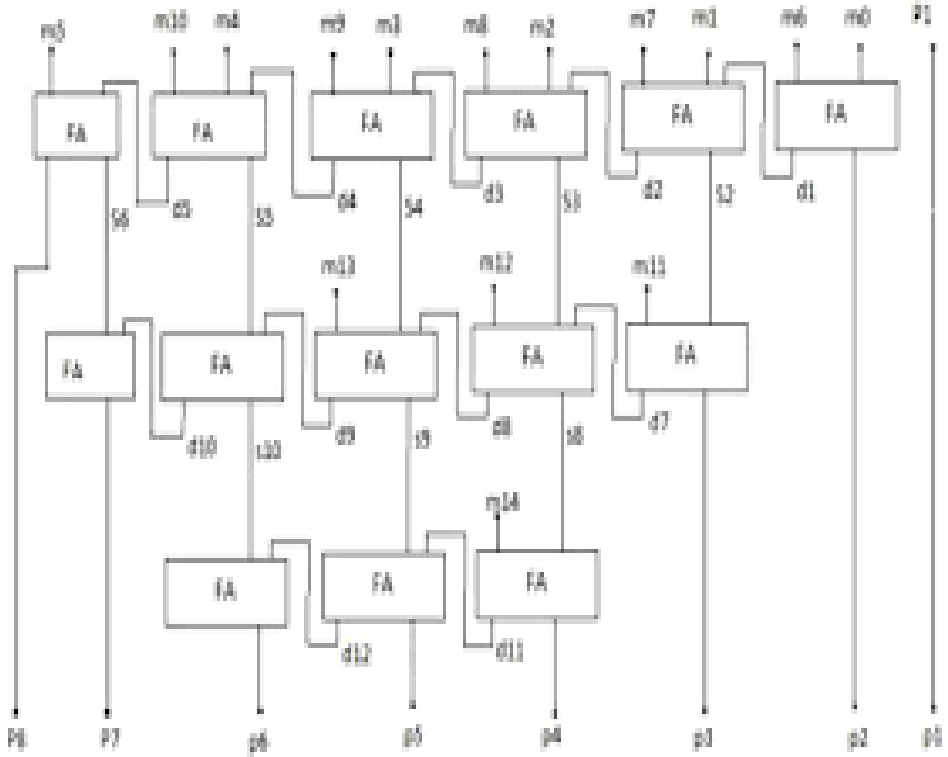

Figure 3*.4x4 Dadda Multiplier using RCA [30]*

Dual channel multiplier [3] using 90nm CMOS technology with serial-parallel schemes. Serial and parallel algorithms and the two main algorithm

which are adopted to improve the performance of multiplier [3].Various types of multipliers are proposed with the booth algorithm multiplication [3] when multiplication is implemental on hardware high amount of power consumed by the process and area is highly considerable [3]Size of operand leads to the size of hardware.

Designing the approximate4-2 compressor can lead the high performance, low power consumption and power efficient circuits. Modifications in the previous design [26] leads additional accuracy. Consumption of less power, less area or less hardware requirement and error recovery module.

Practically Approximate Multiplier have application in the field of image processing , image sharpening which leads in the multimedia fields[26].Error Tolerant Application, such as Data Analysis , data mining pattern recognition, multimedia processing Approximate, logarithmic Multiplier[1].

2. Emerging trends:

In this section, a brief survey study is presented based on the Architecture of various multiplier and their performance parameters in MAC unit and Digital signal processing Applications.

Approximate Booth multipliers are designed based on ap-proximate radix-4 modified Booth encoding (MBE) algorithms and a regular partial product array that employs an approximate Wallace tree. Two approximate Booth encoders are discussed and analyzed for error-tolerant computing. The error characteristics are analyzed with respect to the so-called approximation factor that is related to the inexact bit width of the Booth multipliers [10].

Approximate Multiplier 4-2 Compressor design modified with Carry recovery module. It is highly accurate, consumes less power and require less hardware[26].

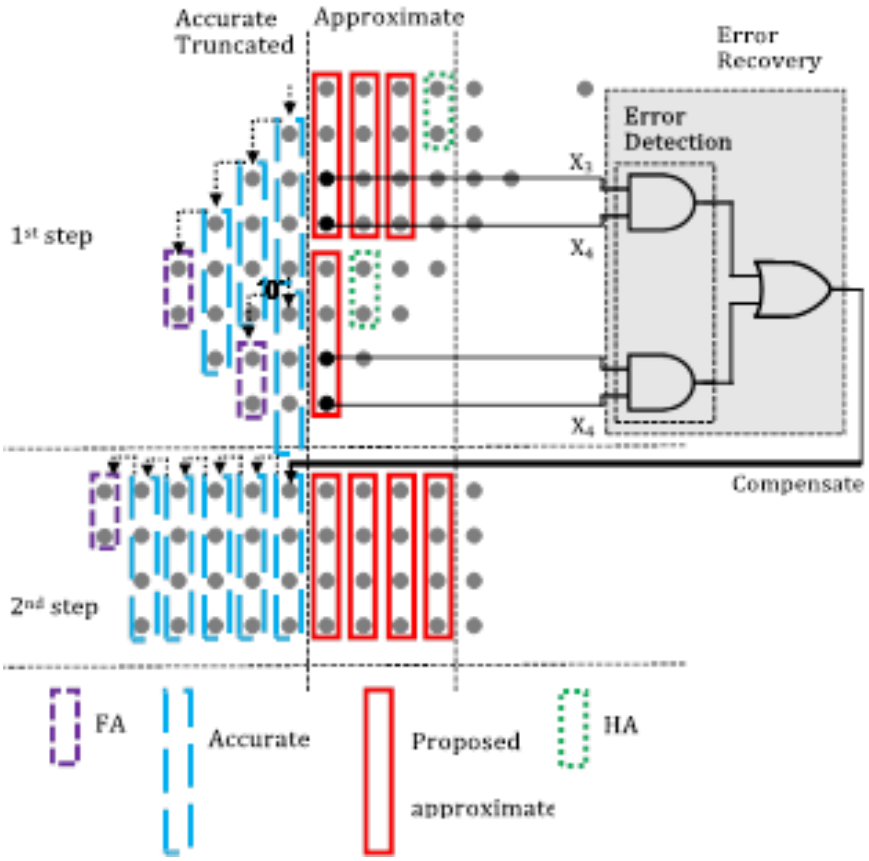

Figure 3 *Partial product accumulation process using truncation and proposed approximate compressors for an 8-bit approximate multiplier with error detection module and error recovery module.[26]*

In this Approxiamate Multiplier Partial Product Accumulation is categories into three steps:

1. 7 bit accurate region. (OR Gate is used to produce Carryto LSB at this Region)
2. 4 bit Approximate region
3. 4 bit Truncated Region

Error Deection and Error recovery is done at the MSB Portion[26]. Following Equations are propsed by auther for sum and carry.

$$C' \square X_1 \square X_2 \square X_1 \square X_3 \square X_1 \square X_4 \square X_2 \square X_3 \square X_2 \square X_4 .$$

$$S' \square (X_1 \square X_2) \square (X_3 \square X_4), [26]$$

3. Conclusion:

Approxiamate multipliers have application Machine learning, Digital Signal Processor (DSP), Image Processing and image sharpening. Error Minimization is the main Constraint during the analysis of Approximate multiplier. Main Parameters considered to reduce the power, size and area of multiplier. Different Researchers uses various techniques and tools to for optimizazation technique for various Multipliers.

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